IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Darren L. Anand, et al.

Examiner: James C. Kerveros

Serial No: 10/707,071

Art Unit: 2117

Filed: November 19, 2003

Docket: BUR920030168US1 (17124)

For: AUTOMATIC BIT FAIL MAPPING FOR EMBEDDED MEMORIES WITH CLOCK MULTIPLIERS

Date: June 17, 2008

Confirmation No: 1070

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with 37 C.F.R §§1.97 and 1.98, it is requested that the following references, which are also listed on the attached Form PTO-1449, be made of record in the above-identified case.

1. U.S. Patent No. 6,255,836, dated July 3, 2001, issued to Schwarz, et al.; and
2. Japanese Patent No. JP 2002-298598A, dated November 10, 2002;

CERTIFICATE OF ELECTRONIC FILING

I hereby certify that this correspondence is being deposited with the United States Patent & Trademark Office via Electronic Filing through the United States Patent and Trademark Office e-business website, on the date shown below.

Dated: June 17, 2008

Steven Fischman

The references were cited in an Official Action dated May 9, 2008, received from the Chinese Patent Office. Applicants are submitting a copy of the above-cited Japanese Patent No. JP 2002-298598A required by 37 C.F.R. 1.98 (a)(2)(i) and (ii).

Further, the undersigned hereby states that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

Inasmuch as this Information Disclosure Statement is being submitted in accordance with the schedule set out in 37 C.F.R.§ 1.704(d), a statement is attached.

Respectfully submitted,

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